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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,337	12/26/2001	Steven K. Hsu	42390.P12624	1975

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EXAMINER
YOHA, CONNIE C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,337	HSU ET AL.	
	Examiner	Art Unit	
	Connie c. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *11-21* is/are allowed.

6)☒ Claim(s) *1- 3, 5, 7,* is/are rejected.

7)☐ Claim(s) *4,6 and 8-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-22 are presented for examination.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claim 5-22 been renumbered 4-21.

Claim Rejections - 35 USC § 112

3. Claim 1, 3 and 5 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is vague and not clear in the claim, therefore can not be understood by the examiner what is meant on line 3 of claim 1, line 9 and 12 of claim 3, and line 9 and 12 of claim 5 "provide a stack effect". Examiner cannot determine by this claim language what or how the stack effect is achieved when a foot transistor coupled to the set of memory cells. Is the memory cells physically or electrically stack on top of the foot transistor is considered causing the stack effect.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of

paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Horiguchi et al, Pat. No. 6339358.

With regard to claim 1, as far as understood, Horiguchi discloses a set of memory cells to store read data (fig. 11, 30); and a foot transistor coupled to the set of memory cells to provide a stack effect (fig. 11, 47X) (col. 11, 41-51) (col. 14, line 60-67)(abstract).

With regard to claim 2, Horiguchi discloses wherein the foot transistor is ON during a read operation (operable state) on one of the memory cells, and wherein the foot transistor is OFF (standby state or operation stop state) when no read operation is performed on any of the memory cells (col. 11, line 41-48) (col. 15, line 42-47) (col. 16, line 39-44).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ciraula et al, Pat. No. 6025741.

With regard to claim 7, Ciraula discloses a bitline (fig. 5, 84)); a set of memory cells (fig. 5, 72 or 74) (col. 5, line 19-22) with an inherent read-select transistor, an inherent read-pass transistor used to access and transfer data in and out of the memory device. Ciraula further discloses a foot transistor connected to the memory cells (fig. 5, 88), wherein the foot transistor is ON during a read operation on one of the memory cells, and wherein the foot transistor is OFF when there is no read operation on any of the memory cells (col. 6, line 5-36). Ciraula does not disclose the circuitry having a read-select transistor having a drain connect to the bit line and a source connected to the drain of the read-pass transistor; and a foot transistor having a drain connected to the source of each read-pass transistor. However, it is obvious for an ordinary skill in the art at the time the invention was to recognize that it is a matter of design choice to have such arrangement and connectivity, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70. .

Allowable Subject Matter

6. Claim 3-6 are is objected as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph and rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 8-10 are objected as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 11-21 are allowed.

The prior art of record does not show the limitation of said control circuit includes a read-select port, a read-pass transistor to provide a low impedance path between the read-access transistor and the foot transistor I the memory cell stores a first logical state, and to provide a high impedance path between the read-access transistor and the foot transistor if the memory cell stores a second logical state; wherein the foot transistor and the read-access transistor provide a stack effect if the memory cell stores the first logical stat and the read-access transistor and the foot transistor are OFF; and wherein the foot transistor and the read-pass transistor provide a stack effect if the memory cell stores the second logical state and the foot transistor is OFF. Furthermore, the prior art does not disclose a plurality of foot transistors in one-to-one correspondence with the subsets of memory cells wherein the foot transistor connected to the read-pass transistor in the particular subset of the memory cells is ON, where a foot transistor is OFF if connected to a subset of memory cells in which no read operation is performed.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Assaderaghi et al (6433587) and Noguchi (6054730) disclose a memory device.

8. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

C. Yoha

January 2003

David Nelms
Supervisory Patent Examiner
Technology Center 2800